In the Claims

Claim 1 (previously presented): A method of forming a semiconductor structure, comprising:

providing a semiconductor substrate having a first doped semiconductor region and a second doped semiconductor region over the first doped semiconductor region, one of the first and second doped semiconductor regions being a p-type region and the other being an n-type region;

forming a trench extending through the second doped semiconductor region and into the first doped semiconductor region, the trench having a sidewall comprising the first and second doped semiconductor regions;

forming a first electrically insulative material within the trench to partially fill the trench, the partially-filled trench being filled to above an elevational level of an uppermost portion of the first doped semiconductor region along the sidewall;

forming a metal-containing layer within the partially-filled trench and along the second doped semiconductor region of the sidewall;

reacting at least some of the metal from the metal-containing layer with the second doped semiconductor region of the sidewall to form a silicide from the trench sidewall, the silicide being within the second doped semiconductor region and not within the first doped semiconductor region; and

forming a second electrically insulative material within the trench to cover the silicide.

Claim 2 (canceled).

Claim 3 (previously presented): The method of claim 1 wherein the metal-containing layer comprises one or more of Co, Ni, Ta, W and Ti.

Claim 4 (previously presented): The method of claim 1 wherein the first and second electrically insulative materials are the same as one another in chemical composition.

Claim 5 (original): The method of claim 4 wherein the first and second electrically insulative materials both comprise silicon dioxide.

Claim 6 (original): The method of claim 4 wherein the first and second electrically insulative materials both consist of silicon dioxide.

Claim 7 (original): The method of claim 1 wherein the first doped semiconductor region is the p-type region.

Claim 8 (original): The method of claim 1 wherein the first doped semiconductor region is the n-type region.

Claim 9 (original): The method of claim 1 wherein the first and second doped semiconductor regions comprise conductively-doped silicon.

Claim 10 (original): The method of claim 1 wherein the first and second doped semiconductor regions comprise conductively-doped monocrystalline silicon.

Claim 11 (original): The method of claim 1 wherein the first and second doped semiconductor regions consist essentially of conductively-doped monocrystalline silicon.

Claim 12 (original): The method of claim 1 wherein the first and second doped semiconductor regions consist of conductively-doped monocrystalline silicon.

Claim 13 (original): The method of claim 1 further comprising incorporating the silicide into a bitline.

Claim 14 (currently amended): A method of forming a semiconductor structure, comprising:

providing a semiconductor material having an upper surface;

providing a trench within the semiconductor material, the trench ~~extending therein~~ extending through said upper surface of the semiconductor material;

forming a first electrically insulative material within a bottom portion of the trench to partially fill the trench, the partially-filled trench having a sidewall comprising the semiconductor material;

incorporating the semiconductor material of the sidewall into a silicide, the silicide being a line extending along the sidewall of the trench and the silicide not extending over the upper surface of the semiconductor material; and

filling the trench with a second electrically insulative material to cover the silicide.

Claim 15 (original): The method of claim 14 further comprising incorporating the silicide line into a bitline.

Claim 16 (original): The method of claim 14 further comprising:

forming a metal-containing layer over the substrate, within the partially-filled trench and along the sidewall; and

forming the silicide from metal of the metal-containing layer by reacting metal from the metal-containing layer with the semiconductor material of the sidewall.

Claim 17 (original): The method of claim 14 further comprising:

forming a metal-containing layer over the substrate, within the partially-filled trench and along the sidewall;

forming the silicide from metal of the metal-containing layer by reacting some of the metal from the metal-containing layer with the semiconductor material of the sidewall, some of the metal of the metal-containing layer not reacting to form the silicide; and

removing the unreacted metal of the metal-containing layer.

Claim 18 (original): The method of claim 14 wherein:

the semiconductor material comprises a first doped region and a second doped region over the first doped region;

one of the first and second doped regions is a p-type region and the other is an n-type region;

the trench extends entirely through the second doped region and has a portion extending within the first doped region; and

the first electrically insulative material entirely fills the portion of the trench that is within the first doped region.

Claim 19 (original): The method of claim 18 wherein the first doped region is the n-type region.

Claim 20 (original): The method of claim 18 wherein the first doped region is the p-type region.

Claim 21 (original): The method of claim 14 wherein the first and second electrically insulative materials are the same as one another in chemical composition.

Claim 22 (original): The method of claim 14 wherein:

said sidewall is one of a pair of opposing sidewalls within the partially-filled trench;

the silicide line is a first silicide line;

semiconductor material of the other of said pair of opposing sidewalls is incorporated into a silicide to form a second silicide line extending along the trench; and

the second silicide line is spaced from the first silicide line.

Claims 23-101 (canceled).